MANSOURA UNIVERSITY
FACULTY OF ENGINEERING
DEPT. OF ELECT. & COMM. ENG.

Jan. 2009
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Total Mark 80

2nd. YEAR COMM. ENG.
LOGIC CIRCUITS (2)
TIME ALLOWED = 3 HRS

Answer ALL Questions

I-a) A sequential circuit has one J-K flip flop with output A and one D-flip flop with output B, one input Y, and one output Z. The flip flops and output equations are as follows:

$$J_A = BY + \overline{B} \quad , \quad K_A = \overline{B}Y \quad , \quad D_B = \overline{A}Y \quad , \quad Z = AY + B\overline{Y}$$

i- Draw the logic diagram of the circuit, ii- Derive the state table, iii- Draw the state diagram.

b) Given the state diagram shown in Fig.1, design and implement the corresponding sequential circuit using J-K flip flops.

II-a)Excess-3 code is generated by adding 3 to the BCD code. State a truth table showing the decimal digits 1, 2, 3,........9, the corresponding BCD code, and the corresponding excess-3 code.

i-Design a combinational logic circuit that converts a 4-bit BCD input to its corresponding 4-bit excess-3 output. Implement your design using discrete AND, OR, XOR, and INVERTER gates.

ii-Implement the BCD-to-Excess-3 code converter in part (i) using programmable logic array (PLA) with 4-inputs and 4-outputs.

b)A BCD-to-Seven segment decoder is a combinational circuit that accepts a decimal digit in BCD and generates the appropriate outputs for selection of segments in a display indicator displaying the decimal digit as shown in Fig.2. State a truth table for BCD-to-Seven segment decoder. Design and implement the corresponding combinational circuit using:

i- A 16x7 ROM

ii- A programmable array logic (PAL) consisting of 4-inputs, 7-outputs, 7-sections each consisting of four-wide AND-OR array. One of the outputs is feed back to input.

III-a)Derive the synchronous input equations of a 4-bit synchronous binary counter based on D-type flip flops. Draw the corresponding counter circuit with the provision of Count Enable connection.

b)Design a combinational circuit that compares two 4-bit numbers A and B to check if they are equal. The circuit has one output Y so that Y=1 if A=B and Y=0 if A is not equal to B. Implement your design using discrete logic gates.

IV-a)Some microprocessors do not provide a separate address bus, instead they use the data bus for address transmission by multiplexing. With the aid of graphical illustration explain the multiplexed bus configuration system.

b) In a certain µP, the main program runs from address D110 to D193. Four nested subroutines have their start and end addresses as:

subroutine A→ A200 to A235
subroutine B→ A239 to A258
subroutine C→ C1A1 to C1A9
subroutine D→ C239 to C258

The BRANCH instructions are at the following addresses:

subroutine A→ D122
subroutine B→ A232
subroutine C→ A249

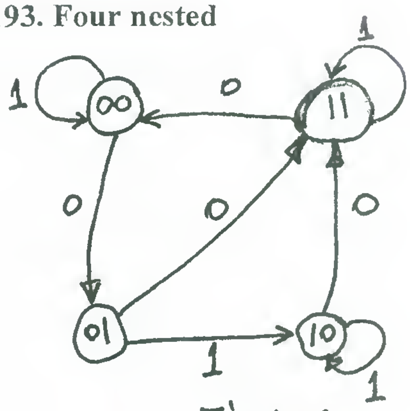

Fig.1

اقلب الصفحة من فضلك

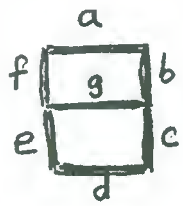

Fig.2

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subroutine D→ C1A4

i-If the CPU internal stack registers are used, graphically show what the stack registers will contain after each push and pop operation.

ii-If a memory type stack whose addresses run from B138 to B13D (6-deep stack) is used. Graphically show the contents of the stack, the stack pointer, and program counter after all branches and returns for all four subroutines.

V-a)In a certain µP the effective addresses of some locations in data memory are pre-stored in scratch pad locations as follows:

Memory address	Scratch pad address
112B	02
13AC	03
146E	04
003A	05
003B	06
003C	07

The data for operands A, B, and C are stored in the locations: A in location 112B, B in location 13AC, and C in location 146E. Write a program using the codes given in the tables attached to first clear the accumulator, then perform the following operations using the previously cleared accumulator, and Indirect addressing Mode:

1. A+B=W, and W to be stored in the memory location 003A
2. W-C=X, and X to be stored in the memory location 003B
3. X+W=Z, and Z to be stored in the memory location 003C

b)The accumulator of a certain µP contains 35_H. The location to be accessed in the data memory contains 54_H. The instruction which uses the program counter relative addressing mode, is fetched from address 0554_H of the program memory. The A field of the instruction contains 81_H. The O field of the instruction commands the µP to transfer the contents of the accessed data memory location into the accumulator and add it to the previous contents.

i- Determine the contents of instruction register, the program counter after the instruction is fetched, the MAR, and the accumulator after the instruction is executed.

ii- If the programmer by mistake inserted 71_H in the A field of the instruction instead of 81_H. Repeat part (i) showing the effect of this error.

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Table 5-3 THE M-FIELD CODES FOR THE GEMINI-A INSTRUCTIONS

Binary	*HEX*	*Instructions*
0000	0	Direct addressing
0001	1	Indirect addressing through scratch pad
0010	2	Indirect addressing through base page (Page 0)
0011	3	Page relative addressing (current page)
0100	4	Base page relative addressing
0101	5	Program counter relative addressing
0110	6	Immediate addressing (2-word instruction)
0111	7	Direct index addressing (2-word instruction)
1000	8	Indirect indexed addressing
1001	9	Indexed indirect addressing
1111	F	Nonmemory reference instruction—A field of the instruction i

Table 5-2 THE O-FIELD CODES FOR THE GEMINI-A INSTRUCTIONS

Binary	*HEX*	*Instruction*
0001	1	Store, (ACC) → MEM
0010	2	Load, (MEM) → ACC and add (MEM) + (ACC) → ACC
0011	3	Load, (MEM) → ACC and subtract (ACC) − (MEM) → ACC
0100	4	Clear ACC
0101	5	Load index register (if the M code is the immediate address mode second word of that instruction will be loaded into the index regis
0110	6	Load scratch pad immediately. The address of the scratch-pad reg will be given in the A field of the instruction, and the operand to loaded will be in the second word of the instruction.
0111	7	JUMP, unconditional